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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/30/2003

Philippe Diehl

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EXAMINER

CHRISS, ANDREW W

ART UNIT

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2619

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DELIVERY MODE

05/02/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/673,665	Applicant(s) DIEHL ET AL.	
	Examiner Andrew Chriss	Art Unit 2619	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 February 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-4,9-14 and 20-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4,9-14 and 20-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. Applicant's amendment, filed February 11, 2008, has been entered and carefully considered. Claims 2-4 and 10-14 have been amended, Claims 5-8, 15-19, and 25-27 have been cancelled, and Claims 1-4, 9-14, and 20-24 are currently pending.
2. In light of Applicant's amendment to Claims 2-4 and 10-14, rejection of said claims under 35 U.S.C. 112, second paragraph, is withdrawn.

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
4. **Claims 1-3, 9-13, and 20-24** rejected under 35 U.S.C. 103(a) as being unpatentable over Reblewski et al (United States Patent 6,265,894), hereinafter Reblewski, in view of Kappler et al (United States Patent 6,064,677), hereinafter Kappler.

Regarding Claims 1 and 9, Reblewski teaches a reconfigurable integrated circuit for use in an emulation system (column 1, line 66 – column 2, line 2). However, Reblewski does not teach a storage unit comprising a signal inclusion schedule or circuitry operative to generate and transmit a message. In the same field of endeavor, Kappler teaches a calendar queue mechanism for scheduling transport of units or cells, specifically high frequency/high priority flows and low frequency/low priority flows (column 12, line 65 – column 13, line 10). Further, Kappler teaches a set of transmit lists 65, connected to calendar queue 63 (Figure 3), which generate and transmit the messages released by the calendar queue (column 11, lines 25-30). As mentioned

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above, the calendar queue specifies the frequency of the signals to include. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the scheduling and transmission taught in Kappler on the reconfigurable emulation integrated circuit taught in Reblewski in order to reduce relative data transport unit delay variations in time-multiplexed outputs from output queued routing mechanisms.

Regarding Claims 2 and 10, Reblewski and Kappler teach all of the limitations of Claims 1 and 9, as described above. However, Reblewski does not teach signals determined to be more critical transmitted more frequently. In the same field of endeavor, Kappler further teaches flows having different frequencies are prioritized so that the data transport units of the higher frequency flows are given transmit priority over any data transport units of lower frequency flows with which they happen to collide (column 12, lines 30-37). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the scheduling and transmission taught in Kappler on the reconfigurable emulation integrated circuit taught in Reblewski in order to reduce relative data transport unit delay variations in time-multiplexed outputs from output queued routing mechanisms.

Regarding Claim 3 and 12, Reblewski and Kappler teach all of the limitations of Claims 1 and 9, as described above. However, Reblewski does not teach generating and transmitting a message in a plurality of clock cycles of an operating clock independent of an emulation clock. In the same field of endeavor, Kappler further teaches that the calendar queue 63 implements a stalled virtual clock so that cells that are scheduled for transmission are leased for transmission only when system “real time” has reached their respective scheduled transmission times (column 11, lines 21-25). Therefore, messages are generated in a plurality of clock cycles of an operating

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clock independent of the predetermined rate of the overall system clock (column 8, lines 53-59). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the scheduling and transmission taught in Kappler on the reconfigurable emulation integrated circuit taught in Reblewski in order to reduce relative data transport unit delay variations in time-multiplexed outputs from output queued routing mechanisms.

Regarding Claim 11, Reblewski and Kappler teach all of the limitations of Claim 9, as described above. However, Reblewski does not teach the message comprising state values. In the same field of endeavor, Kappler teaches that each outbound message contain VP and VC identifiers (Figure 2), equivalent to Applicant's disclosed state value (Figure 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the scheduling and transmission taught in Kappler on the reconfigurable emulation integrated circuit taught in Reblewski in order to reduce relative data transport unit delay variations in time-multiplexed outputs from output queued routing mechanisms.

Regarding Claim 13, Reblewski and Kappler teach all of the limitations of Claim 9, as described above. However, Reblewski does not teach extracting a parity value from a message. In the same field of endeavor, Kappler teaches reading a CRC (parity) value from an inbound cell (Figure 2). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the scheduling and transmission taught in Kappler on the reconfigurable emulation integrated circuit taught in Reblewski in order to reduce relative data transport unit delay variations in time-multiplexed outputs from output queued routing mechanisms.

Regarding Claim 20, Reblewski teaches an integrated circuit for use in an emulation system, as described with regards to Claims 1 and 9. Reblewski further teaches multiple reconfigurable logic resources (Figure 2), output pins 113, and a partial scan register that receives a plurality of output signals from logic elements (column lines 6-15), equivalent to Applicant's claimed message formation and send block. However, Reblewski does not teach a signal inclusion schedule. In the same field of endeavor, Kappler teaches a signal inclusion schedule, as discussed with regards to Claims 1 and 9. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the scheduling and transmission taught in Kappler on the reconfigurable emulation integrated circuit taught in Reblewski in order to reduce relative data transport unit delay variations in time-multiplexed outputs from output queued routing mechanisms.

Regarding Claim 21, Reblewski teaches an input pin 113. Reblewski further teaches a logic element that receives multiple inputs and outputs a single signal (truth table 202). However, Reblewski does not teach the claimed message receive and disassembly block nor the signal inclusion schedule. In the same field of endeavor, Kappler teaches a switching fabric that decomposes cells into four bit wide "nibbles" for arbitration and routing (column 10, lines 7-13), equivalent to Applicant's claimed message received and disassembly block. Kappler further teaches a signal inclusion schedule, as discussed with regards to Claims 1 and 9. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the scheduling and transmission taught in Kappler on the reconfigurable emulation integrated circuit taught in Reblewski in order to reduce relative data transport unit delay variations in time-multiplexed outputs from output queued routing mechanisms.

Regarding Claim 22, Reblewski teaches a plurality of output pins 113. Further, Reblewski teaches an array of reconfigurable integrated circuits in Figure 10, thereby teaching multiple partial scan registers.

Regarding Claim 23, Reblewski teaches an array of reconfigurable integrated circuits in Figure 10, thereby teaching a plurality of reconfigurable logic resources in communication with the message formation and send block.

Regarding Claim 24, Reblewski teaches an integrated circuit for use in an emulation system, as described with regards to Claims 1, 9, and 20. Reblewski further teaches multiple reconfigurable logic resources (Figure 2) and input pins 113. However, Reblewski does not teach the claimed message receive and disassembly block nor the signal inclusion schedule. In the same field of endeavor, Kappler teaches a switching fabric that decomposes cells into four bit wide “nibbles” for arbitration and routing (column 10, lines 7-13), equivalent to Applicant’s claimed message received and disassembly block. Kappler further teaches a signal inclusion schedule, as discussed with regards to Claims 1 and 9. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the scheduling and transmission taught in Kappler on the reconfigurable emulation integrated circuit taught in Reblewski in order to reduce relative data transport unit delay variations in time-multiplexed outputs from output queued routing mechanisms.

5. **Claims 4 and 14** rejected under 35 U.S.C. 103(a) as being unpatentable over Reblewski in view of Kappler as applied to claims 1 and 13 above, and further in view of Sindhushayana et al (United States Patent Application Publication US 2003/0053435 A1), hereinafter Sindhushayana. Reblewski and Kappler teach all of the limitations of Claims 1 and 13, as

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discussed above. However, the references do not teach a parity bit generator. In the same field of endeavor, Sindhushayana teaches a channel interleaver that permutes systematic bits with parity bits, thus generating a parity value and transmitting a message containing a parity value. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the parity value generator taught in Sindhushayana with the reconfigurable emulation integrated circuit taught in Reblewski, as modified above, in order to employ an error correction system that overcomes the impact of interference in a wireless system.

Response to Arguments

6. Applicant's arguments with respect to rejection of Claims 1-3, 9-13, and 20-24 under 35 U.S.C. 103(a) have been fully considered but they are not persuasive. Applicant states that Kappler fails to teach or suggest a signal inclusion schedule that specifies the order and the frequency of occurrence of the plurality of signals in the message. Applicant further states that Kappler uses the word "frequency" to describe data frequency with respect to bandwidth, where higher data flows are given transmit priority over lower data frequency flows. However, Kappler discloses a calendar queue mechanism for scheduling transport of units or cells, specifically high frequency/high priority flows and low frequency/low priority flows (column 12, line 65 – column 13, line 10). Data flow prioritization is performed on the basis of a specified frequency, or expected/negotiated emission intervals (column 12, lines 56-64). Therefore, it clear to one of ordinary skill in the art that the calendar queue mechanism disclosed in Kappler comprises information regarding the frequency of occurrence of the plurality of signals in the message. Therefore, rejection of Claims 1-3, 9-13, and 20-24 under 35 U.S.C. 103(a) is maintained.

7. Applicant's arguments with respect to rejection of Claims 4 and 14 under 35 U.S.C. 103(a) have been fully considered but they are not persuasive. Applicant states that Sindhushayana fails to remedy the deficiencies of Reblewski and Kappler with respect to Claims 1 and 9, from which Claims 4 and 14 depend. However, as described above, Reblewski and Kappler disclose all of the limitations of Claims 1 and 9. Therefore, rejection of Claims 4 and 14 under 35 U.S.C. 103(a) is maintained.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Chriss whose telephone number is (571)272-1774. The examiner can normally be reached on Monday - Friday, 7:30 AM - 5:00 PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau Nguyen can be reached on 571-272-3126. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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